ABSTRACT

Processes, software and systems asymmetrically shrink a layout for a VLSI circuit design. A first VLSI circuit design layout, defined by a first fabrication process with first design rules, is asymmetrically scaled to a second VLSI circuit design layout defined by a second fabrication process with second design rules. Layouts of one or more leaf cells of the second VLSI circuit design layout are processed to ensure conformity to the second design rules.